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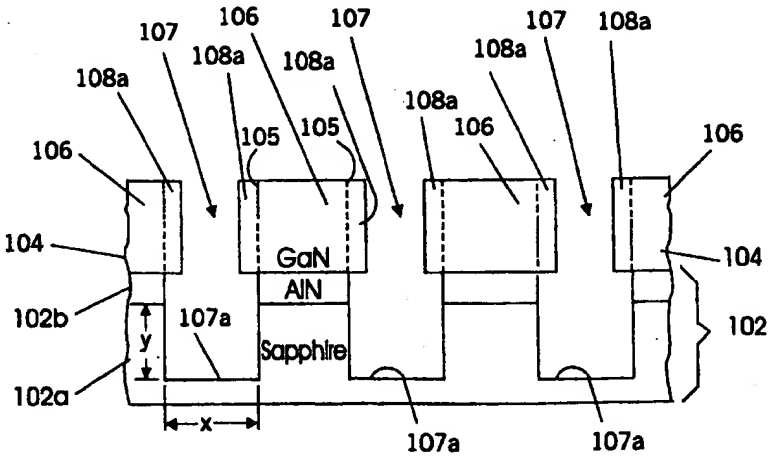

(57) Abstract: Gallium nitride semiconductor layers may be fabricated by etching an underlying gallium nitride layer (104) on a sapphire substrate (102a), to define at least one post (106) in the underlying gallium nitride layer and at least one trench (107) in the underlying gallium nitride layer. The at least one post includes a gallium nitride top and a gallium nitride sidewall (105). The at least one trench includes a trench floor. The gallium nitride sidewalls are laterally grown into the at least one trench, to thereby form a gallium nitride semiconductor layer. In a preferred embodiment, the at least one trench extends into the sapphire substrate such that the at least one post further includes a sapphire sidewall an a sapphire floor. A mask (201) may be included on the sapphire floor and an alluminum nitride buffer layer (102b) also may be included between the sapphire substrate and the underlying gallium nitride layer. A mask (209) also may be included on the gallium nitride top. The mask on the floor and the mask on the top preferably comprise same material.

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PENDEOEPITAXIAL GROWTH OF GALLIUM NITRIDE LAYERS ON SAPPHIRE SUBSTRATES

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Field of the Invention

This invention relates to microelectronic devices and fabrication methods, and more particularly to gallium nitride semiconductor devices and fabrication methods therefor.

Background of the Invention

Gallium nitride is being widely investigated for microelectronic devices including but not limited to transistors, field emitters and optoelectronic devices. It will be understood that, as used herein, gallium nitride also includes alloys of gallium nitride such as aluminum gallium nitride, indium gallium nitride and aluminum indium gallium nitride.

A major problem in fabricating gallium nitride-based microelectronic devices is the fabrication of gallium nitride semiconductor layers having low defect densities. It is known that one contributor to defect density is the substrate on which the gallium nitride layer is grown. Accordingly, although gallium nitride layers have been grown on sapphire substrates, it is known to reduce defect density by growing gallium nitride layers on aluminum nitride buffer layers which are themselves formed on silicon carbide substrates. Notwithstanding these advances, continued reduction in defect density is desirable.

It also is known to produce low defect density gallium nitride layers by forming a mask on a layer of gallium nitride, the mask including at least one opening

therein that exposes the underlying layer of gallium nitride, and laterally growing the underlying layer of gallium nitride through the at least one opening and onto the mask. This technique often is referred to as "Epitaxial Lateral Overgrowth" (ELO). The layer of gallium nitride may be laterally grown until the gallium nitride coalesces on the mask to form a single layer on the mask. In order to form a continuous layer of gallium nitride with relatively low defect density, a second mask may be formed on the laterally overgrown gallium nitride layer, that includes at least one opening that is offset from the opening in the underlying mask. ELO then again is performed through the openings in the second mask to thereby overgrow a second low defect density continuous gallium nitride layer. Microelectronic devices then may be formed in this second overgrown layer. ELO of gallium nitride is described, for example, in the publications entitled *Lateral Epitaxy of Low Defect Density GaN Layers Via Organometallic Vapor Phase Epitaxy* to Nam et al., Appl. Phys. Lett. Vol. 71, No. 18, November 3, 1997, pp. 2638-2640; and *Dislocation Density Reduction Via Lateral Epitaxy in Selectively Grown GaN Structures* to Zheleva et al, Appl. Phys. Lett., Vol. 71, No. 17, October 27, 1997, pp. 2472-2474, the disclosures of which are hereby incorporated herein by reference.

It also is known to produce a layer of gallium nitride with low defect density by forming at least one trench or post in an underlying layer of gallium nitride to define at least one sidewall therein. A layer of gallium nitride is then laterally grown from the at least one sidewall. Lateral growth preferably takes place until the laterally grown layers coalesce within the trenches. Lateral growth also preferably continues until the gallium nitride layer that is grown from the sidewalls laterally overgrows onto the tops of the posts. In order to facilitate lateral growth and produce nucleation of gallium nitride and growth in the vertical direction, the top of the posts and/or the trench floors may be masked. Lateral growth from the sidewalls of trenches and/or posts also is referred to as "pendeoepitaxy" and is described, for example, in publications entitled *Pendeo-Epitaxy: A New Approach for Lateral Growth of Gallium Nitride Films* by Zheleva et al., Journal of Electronic Materials, Vol. 28, No. 4, February 1999, pp. L5-L8; and *Pendeoepitaxy of Gallium Nitride Thin Films* by Linthicum et al., Applied Physics Letters, Vol. 75, No. 2, July 1999, pp. 196-198, the disclosures of which are hereby incorporated herein by reference.

ELO and pendeoepitaxy can provide relatively large, low defect gallium nitride layers for microelectronic applications. However, a major concern that may

limit the mass production of gallium nitride devices is the growth of the gallium nitride layers on a silicon carbide substrate. Notwithstanding silicon carbide's increasing commercial importance, silicon carbide substrates still may be relatively expensive. Moreover, it may be difficult to use silicon carbide substrates in optical devices, where back illumination may be desired, because silicon carbide is opaque Accordingly, the use of an underlying silicon carbide substrate for fabricating gallium nitride microelectronic structures may adversely impact the cost and/or applications of gallium nitride devices.

Summary of the Invention

The present invention pendeoepitaxially grows sidewalls of posts in an underlying gallium nitride layer that itself is on a sapphire substrate, by treating the underlying gallium nitride layer and/or the sapphire substrate to prevent vertical growth of gallium nitride from the trench floor from interfering with the pendeoepitaxial growth of the gallium nitride sidewalls of the posts. Thus, widely available sapphire substrates may be used for pendeoepitaxial of gallium nitride, to thereby allow reduced cost and/or wider applications for gallium nitride devices.

More specifically, gallium nitride semiconductor layers may be fabricated by etching an underlying gallium nitride layer on a sapphire substrate, to define at least one post in the underlying gallium nitride layer and at least one trench in the underlying gallium nitride layer. The at least one post includes a gallium nitride top and a gallium nitride sidewall. The at least one trench includes a trench floor. The gallium nitride sidewalls are laterally grown into the at least one trench, to thereby form a gallium nitride semiconductor layer. However, prior to performing the laterally growing step, the sapphire substrate and/or the underlying gallium nitride layer is treated to prevent growth of gallium nitride from the trench floor from interfering with the lateral growth of the gallium nitride sidewalls of the at least one post into the at least one trench.

The sapphire substrate may be etched beneath the at least one trench sufficiently deep to create a sapphire floor and to prevent vertical growth of gallium nitride from the sapphire floor from interfering with the lateral growth of the gallium nitride sidewalls of the at least one post into the at least one trench. Alternatively or in addition, the trench floor may be masked with a mask. In yet other alternatives, the underlying gallium nitride layer is selectively etched to expose the sapphire substrate

and create a sapphire floor. The gallium nitride post tops also may be masked to reduce nucleation of gallium nitride thereon, compared to on gallium nitride. Following growth, at least one microelectronic device may be formed in the gallium nitride semiconductor layer.

Even more specifically, an underlying gallium nitride layer on a sapphire substrate is etched to selectively expose the sapphire substrate and define at least one post and at least one trench in the underlying gallium nitride layer. The at least one post each includes a gallium nitride top and a gallium nitride sidewall. The at least one trench includes a sapphire floor. The gallium nitride sidewall of the at least one post is grown laterally into the at least one trench, to thereby form a gallium nitride semiconductor layer.

Preferably, when etching the underlying gallium nitride layer on the sapphire substrate, the sapphire substrate is etched as well, to define at least one post in the underlying gallium nitride layer and in the sapphire substrate, and at least one trench in the underlying gallium nitride layer and in the sapphire substrate. The at least one post each includes a gallium nitride top, a gallium nitride sidewall and a sapphire sidewall. The at least one trench includes a sapphire floor. More preferably, the sapphire substrate is etched sufficiently deep to prevent vertical growth of gallium nitride from the sapphire floor from interfering with the step of laterally growing the gallium nitride sidewalls of the at least one post into the at least one trench. For example, the sapphire sidewall height to sapphire floor width ratio exceeds about 1/4. In another embodiment, the sapphire floor is masked with a mask that reduces nucleation of gallium nitride thereon compared to on sapphire.

In yet other embodiments, the sapphire substrate includes an aluminum nitride buffer layer thereon. During the etching step, the gallium nitride layer and the aluminum nitride buffer layer both are etched to selectively expose the sapphire substrate. In other embodiments, the sapphire substrate also is selectively etched so that the trenches extend into the sapphire substrate.

Lateral growth preferably proceeds pendeoepitaxially by laterally overgrowing the gallium nitride sidewall onto the gallium nitride top, to thereby form a gallium nitride semiconductor layer. Prior to pendeoepitaxial growth, the gallium nitride top may be masked with a mask that reduces nucleation of gallium nitride thereon compared to on gallium nitride.

According to another aspect of the present invention, the trench floor may be masked with a mask, thereby obviating the need to expose the sapphire substrate. Specifically, an underlying gallium nitride layer on a sapphire substrate may be etched to define at least one post in the underlying gallium nitride and at least one trench in the underlying gallium nitride layer. The at least one post includes a top and a sidewall and the at least one trench includes a trench floor. The at least one floor is masked with a mask, and the sidewall of the at least one post is laterally grown into the at least one trench, to thereby form a gallium nitride semiconductor layer. As was described above, the post tops also may be masked. Preferably, the at least one floor and the at least one top are masked simultaneously, for example by performing a directional deposition that forms a mask on the lateral tops and floors, but not on the sidewalls. As also was described above, when an aluminum nitride buffer layer is present, it may be etched to define the posts and trenches, or the mask may be formed on the aluminum nitride buffer layer. In another alternative, the trench floor may be located in the gallium nitride layer itself, and the gallium nitride trench floor may be masked as was described above.

Embodiments of gallium nitride semiconductor structures according to the present invention can include a sapphire substrate and an underlying gallium nitride layer on the sapphire substrate. The underlying gallium nitride layer includes therein at least one post and at least one trench. The at least one post each includes a gallium nitride top and a gallium nitride sidewall. The at least one trench includes a sapphire floor. A lateral gallium nitride layer extends laterally from the gallium nitride sidewall of the at least one post into the at least one trench. In a preferred embodiment, the at least one trench extends into the sapphire substrate such that the at least one post each includes a gallium nitride top, a gallium nitride sidewall and a sapphire sidewall and the at least one trench includes a sapphire floor. The sapphire floor preferably is free of a vertical gallium nitride layer thereon and the sapphire sidewall height to sapphire floor width ratio may exceed about 1/4. A mask may be included on the sapphire floor and an aluminum nitride buffer layer also may be included between the sapphire substrate and the underlying gallium nitride layer. A mask also may be included on the gallium nitride top. The mask on the floor and the mask on the top preferably comprise same material.

Other embodiments of gallium nitride semiconductor structures according to the present invention also can include a sapphire substrate and an underlying gallium

nitride layer on the sapphire substrate. The underlying gallium nitride layer includes therein at least one post and at least one trench. The at least one post includes a gallium nitride top and a gallium nitride sidewall, and the at least one trench includes a trench floor. A mask is included on the at least one trench floor, and the gallium nitride layer extends laterally from the gallium nitride sidewall of the at least one post into the at least one trench. In a preferred embodiment, the trench floor is a sapphire floor. A mask may be provided on a gallium nitride top that preferably comprises the same material as the mask on the trench floor. An aluminum nitride buffer layer also may be provided, as was described above. At least one microelectronic device may be formed in the gallium nitride semiconductor layer.

Accordingly, sapphire may be employed as a substrate for growing gallium nitride semiconductor layers that can have low defect densities. Low cost and/or high availability gallium nitride devices thereby may be provided.

Brief Description Of The Drawings

Figures 1-5 are cross-sectional views of first gallium nitride microelectronic structures during intermediate fabrication steps, according to the present invention.

Figures 6-10 are cross-sectional views of other gallium nitride microelectronic structures during intermediate fabrication steps, according to the present invention.

Figures 11-16 are cross-sectional views of yet other gallium nitride microelectronic structures during intermediate fabrication steps, according to the present invention.

Figures 17-22 are cross-sectional views of still other gallium nitride microelectronic structures during intermediate fabrication steps, according to the present invention.

Detailed Description Of Preferred Embodiments

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like

numbers refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" or "onto" another element, it can be directly on the other element or intervening elements may also be present. Moreover, each embodiment described and illustrated herein includes its complementary conductivity type embodiment as well.

Referring now to Figures 1-5, methods of fabricating gallium nitride semiconductor structures according to embodiments of the present invention now will be described. As shown in Figure 1, an underlying gallium nitride layer **104** is grown on a substrate **102**. The substrate **102** includes a sapphire (Al_2O_3) substrate **102a**, preferably with (0001) (c-plane) orientation, and also preferably includes an aluminum nitride and/or gallium nitride buffer layer **102b**. The crystallographic designation conventions used herein are well known to those having skill in the art, and need not be described further. The gallium nitride layer **104** may be between 0.5 and 2.0μm thick, and may be grown at 1000°C on a low temperature (600°C) aluminum nitride buffer layer and/or a low temperature (500°) gallium nitride buffer layer **102b** that was deposited on the sapphire substrate **102a** in a cold wall vertical and inductively heated metalorganic vapor phase epitaxy system using triethylgallium at 26μmol/min, ammonia at 1500 sccm and 3000 sccm hydrogen diluent. The growth of a gallium nitride layer on a sapphire substrate including an aluminum nitride buffer layer is described in publications entitled *Improvements on the Electrical and Luminescent Properties of Reactive Molecular Beam Epitaxially Grown GaN Films by Using AlN-Coated Sapphire Substrates* to Yoshida et al., Appl. Phys. Lett. 42(5), March 1, 1983, pp. 427-429; *Metalorganic Vapor Phase Epitaxial Growth of a High Quality GaN Film Using an AlN Buffer Layer* to Amano et al., Appl. Phys. Lett., 48(5), February 1986, pp. 353-355; *Influence of Buffer Layers on the Deposition of High Quality Single Crystal GaN Over Sapphire Substrate* to Kuznia et al., J. Appl. Phys. 73(9), May 1, 1993, pp. 4700-4702; *GaN Growth Using GaN Buffer Layer* to Nakamura, Japanese Journal of Applied Physics, Vol. 30, No. 10A, October 1991, pp. L1705-L1707; *The Effect of GaN and AlN Buffer Layers on GaN Film Properties Grown on Both C-Plane and A-Plane Sapphire* to Doverspike et al., Journal of Electronic Materials, Vol. 24, No. 4, 1995, pp. 269-273, the disclosures of which are hereby incorporated herein by reference.

Still referring to Figure 1, the underlying gallium nitride layer **104** includes a plurality of sidewalls **105** therein. It will be understood by those having skill in the

art that the sidewalls **105** may be thought of as being defined by a plurality of spaced apart posts **106**, that also may be referred to as "mesas", "pedestals" or "columns". The sidewalls **105** may also be thought of as being defined by a plurality of trenches **107**, also referred to as "wells" in the underlying gallium nitride layer **104**. The sidewalls **105** may also be thought of as being defined by a series of alternating trenches **107** and posts **106**. Moreover, a single post **106** may be provided, that may be thought of as being defined by at least one trench **107** adjacent the single post. It will be understood that the posts **106** and the trenches **107** that define the sidewalls **105** may be fabricated by selective etching and/or selective epitaxial growth and/or other conventional techniques. Moreover, it will also be understood that the sidewalls need not be orthogonal to the substrate **102**, but rather may be oblique thereto. Finally, it will also be understood that although the sidewalls **105** are shown in cross-section in Figure 1, the posts **106** and trenches **107** may define elongated regions that are straight, V-shaped or have other shapes. As shown in Figure 1, the trenches **107** preferably extend into the buffer layer **102b** and into the substrate **102a**, so that subsequent gallium nitride growth occurs preferentially on the sidewalls **105** rather than on the trench floors.

Referring now to Figure 2, the sidewalls **105** of the underlying gallium nitride layer **104** are laterally grown to form a lateral gallium nitride layer **108a** in the trenches **107**. Lateral growth of gallium nitride may be obtained at 1000-1100°C and 45 Torr. The precursors TEG at 13-39μmol/min and NH_3 at 1500 sccm may be used in combination with a 3000 sccm H_2 diluent. If gallium nitride alloys are formed, additional conventional precursors of aluminum or indium, for example, may also be used. As used herein, the term "lateral" means a direction that is orthogonal to the sidewalls **105**. It will also be understood that some vertical growth on the posts **106** may also take place during the lateral growth from sidewalls **105**. As used herein, the term "vertical" denotes a directional parallel to the sidewalls **105**.

When the sapphire substrate is exposed to the gas phase during growth of gallium nitride, it has been found that gallium nitride can nucleate on the sapphire. Thus, vertical growth of gallium nitride may take place from the sapphire trench floors, that can interfere with lateral growth of the gallium nitride sidewalls into the at least one trench. Alternatively, because of the presence of ammonia, the exposed areas of the surface of the sapphire may be converted to aluminum nitride. Unfortunately, gallium nitride can nucleate well on aluminum nitride, and thereby

allow vertical growth of the gallium nitride from the trench floor, which can interfere with the lateral growth of the gallium nitride sidewalls.

The conversion of the exposed areas of the surface of the sapphire to aluminum nitride may be reduced and preferably eliminated by using a high growth temperature for growing the gallium nitride. For example, a temperature of about 1100°C may be used rather than a conventional temperature of about 1000°C. However, this still may not prevent the nucleation of gallium nitride on the floor of the sapphire substrate.

Referring again to Figure 2, according to the present invention, the sapphire substrate **102a** is etched sufficiently deep to prevent vertical growth of gallium nitride from the sapphire trench floor **107a** from interfering with the step of laterally growing the gallium nitride sidewalls of the at least one post into the at least one trench. For example, the ratio of the sapphire sidewall height **y** to the sapphire floor width **x** may be at least 1/4. Other ratios may be used depending on the vertical to lateral growth rate ratio during gallium nitride growth. Under the conditions described below, the lateral growth rate of gallium nitride can be faster than the vertical growth rate. Under these conditions, and with sufficiently deep trenches, the sidewall growth from the posts can coalesce over the trenches before the vertical gallium nitride growth in the trenches that results from nucleation of gallium nitride on the sapphire substrate can interfere with the lateral growth.

Referring now to Figure 3, continued growth of the lateral gallium nitride layer **108a** causes vertical growth onto the underlying gallium nitride layer **104**, specifically onto the posts **106**, to form a vertical gallium nitride layer **108b**. Growth conditions for vertical growth may be maintained as was described in connection with Figure 2. As also shown in Figure 3, continued vertical growth into trenches **107** may take place at the bottom of the trenches. A void **109** preferably remains between the lateral gallium nitride layer **108a** and the trench floor **107a**.

Referring now to Figure 4, growth is allowed to continue until the lateral growth fronts coalesce in the trenches **107** at the interfaces **108c**, to form a continuous gallium nitride semiconductor layer in the trenches. The total growth time may be approximately 60 minutes. As shown in Figure 5, microelectronic devices **110** may then be formed in the lateral gallium nitride semiconductor layer **108a**. Devices may also be formed in vertical gallium nitride layer **108b**.

Accordingly, in Figure 5, gallium nitride semiconductor structures **100** according to embodiments of the present invention are illustrated. The gallium nitride structures **100** include the substrate **102**. The substrate includes the sapphire substrate **102a** and the aluminum nitride buffer layer **102b** on the sapphire substrate **102a**. The aluminum nitride and/or gallium nitride buffer layer **102b** may be about 200-300Å thick.

The underlying gallium nitride layer **104** is also included on the buffer layer **102b** opposite the substrate **102a**. The underlying gallium nitride layer **104** may be between about 0.5 and 2.0μm thick, and may be formed using metalorganic vapor phase epitaxy (MOVPE). The underlying gallium nitride layer generally has an undesired relatively high defect density. For example, dislocation densities of between about 10^8 and $10^{10}cm^{-2}$ may be present in the underlying gallium nitride layer. These high defect densities may result from mismatches in lattice parameters between the buffer layer **102b** and the underlying gallium nitride layer **104**, and/or other causes. These high defect densities may impact the performance of microelectronic devices formed in the underlying gallium nitride layer **104**.

Still continuing with the description of Figure 5, the underlying gallium nitride layer **104** includes the plurality of sidewalls **105** that may be defined by the plurality of posts **106** and/or the plurality of trenches **107**. As was described above, the sidewalls may be oblique and of various elongated shapes. The posts **106** include a gallium nitride top, a gallium nitride sidewall and a sapphire sidewall, and the at least one trench includes a sapphire floor **107a**. The sapphire floor **107a** preferably is free of a vertical gallium nitride layer thereon. The sapphire sidewall height to sapphire floor width ratio preferably is at least 1/4.

Continuing with the description of Figure 5, the lateral gallium nitride layer **108a** extends from the plurality of sidewalls **105** of the underlying gallium nitride layer **104**. The lateral gallium nitride layer **108a** may be formed using metalorganic vapor phase epitaxy at about 1000-1100°C and 45 Torr. Precursors of triethygallium (TEG) at 13-39μmol/min and ammonia (NH_3) at 1500 sccm may be used in combination with a 3000 sccm H_2 diluent, to form the lateral gallium nitride layer **108a**. The gallium nitride semiconductor structure **100** also includes the vertical gallium nitride layer **108b** that extends vertically from the posts **106**.

As shown in Figure 5, the lateral gallium nitride layer **108a** coalesces at the interfaces **108c** to form a continuous lateral gallium nitride semiconductor layer **108a**

in the trenches. It has been found that the dislocation densities in the underlying gallium nitride layer **104** generally do not propagate laterally from the sidewalls **105** with the same density as vertically from the underlying gallium nitride layer **104**. Thus, the lateral gallium nitride layer **108a** can have a relatively low defect density, for example less that 10^4 cm^{-2}. Accordingly, the lateral gallium nitride layer **108b** may form device quality gallium nitride semiconductor material. Thus, as shown in Figure 5, microelectronic devices **110** may be formed in the lateral gallium nitride semiconductor layer **108a**. It will also be understood that a mask need not be used to fabricate the gallium nitride semiconductor structures **100** of Figure 5, because lateral growth is directed from the sidewalls **105**.

Figures 6-10 illustrate other embodiments according to the present invention. As shown in Figure 6, a mask **201** is formed on the trench floors **107a'**. When forming the mask **201** on the trench floors **107a'**, the trench need not be etched into the sapphire substrate **102a**. Rather, as shown in Figure 6, the trench may only be etched through the aluminum nitride buffer layer **102b**. However, it will be understood by those having skill in the art that the trench also may be etched into the sapphire substrate **102a**, as was illustrated in Figure 1, and the trench floor **107a** in the sapphire substrate may be masked with a mask **201**. In still another alternative, the trench may be etched only partially into the aluminum nitride buffer layer **102b**, rather than entirely through the aluminum nitride buffer layer **102b** as shown in Figure 6. In yet another alternative, the trench need not be etched into the aluminum nitride buffer layer **102b** at all, but rather the mask **201** may be formed on the exposed portion of the aluminum nitride buffer layer **102b**. In yet another alternative, the trenches may not extend into the aluminum nitride buffer layer, but rather may terminate within the gallium nitride layer **104**, and the mask **201** may be formed on the gallium nitride floor. Finally, it will be understood that although the mask **201** is shown to have the same thickness as the aluminum nitride buffer layer **102b**, it need not have the same thickness. Rather, it can be thinner or thicker.

It has been found, according to the present invention, that gallium nitride does not nucleate appreciably on certain amorphous and crystalline materials, such as silicon dioxide, silicon nitride and certain metals such as tungsten. Accordingly, a "line of sight" deposition technique, such as thermal evaporation or electron beam evaporation, may be used to deposit a masking material such as silicon dioxide, silicon nitride and/or tungsten on the trench floors. Since the gallium nitride does not

nucleate specifically on the mask, it can be forced to grow off the sidewalls of the posts only. The remaining processing steps of Figures 6-10 correspond to those of Figures 1-5, and need not be described again herein.

Figures 11-16 illustrate yet other embodiments according to the present invention. In Figures 11-16, the sapphire substrate **102a** is etched sufficiently deep to prevent vertical growth of gallium nitride from the sapphire floor from interfering with the step of laterally growing the gallium nitride sidewalls of the at least one post into the at least one trench, as was described in connection with Figures 1-5, and need not be described herein again. However, in contrast with Figures 1-5, in Figures 11-16, a mask, such as a silicon dioxide, silicon nitride and/or tungsten mask **209** is included on the underlying gallium nitride layer **104**. The mask **209** may have a thickness of about 1000Å or less and may be formed on the underlying gallium nitride layer **104** using low pressure Chemical Vapor Deposition (CVD) of silicon dioxide and/or silicon nitride. Alternatively, electron beam or thermal evaporation may be used to deposit tungsten. The mask **209** is patterned to provide an array of openings therein, using conventional photolithography techniques.

As shown in Figure 11, the underlying gallium nitride layer is etched through the array of openings to define the plurality of posts **106** in the underlying gallium nitride layer **104** and the plurality of trenches **107** therebetween. The posts each include the sidewall **105** and a top having the mask **209** thereon. It will also be understood that although the posts **106** and trenches **107** are preferably formed by masking and etching as described above, the posts may also be formed by selectively growing the posts from an underlying gallium nitride layer and then forming a capping layer on the tops of the posts. Combinations of selective growth and selective etching also may be used.

As shown in Figure 12, the sidewalls **105** of the underlying gallium nitride layer **104** are laterally grown to form a lateral gallium nitride layer **108a** in the trenches **107**. Lateral growth may proceed as was described above. It will be understood that growth and/or nucleation on the top of the posts **106** is reduced and preferably eliminated by the mask **209**.

Referring to Figure 13, continued growth of the lateral gallium nitride layer **108a** causes vertical growth of the lateral gallium nitride layer **108a** through the array of openings. Conditions for vertical growth may be maintained as was described in connection with Figure 12.

Referring now to Figure 14, continued growth of the lateral gallium nitride layer **108a** causes lateral overgrowth onto the mask **209**, to form an overgrown lateral gallium nitride layer **108b**. Growth conditions for overgrowth may be maintained as was described in connection with Figure 12.

Referring now to Figure 15, growth is allowed to continue until the lateral growth fronts coalesce in the trenches **107** at the interfaces **108c**, to form a continuous lateral gallium nitride semiconductor layer **108a** in the trenches.

Still referring to Figure 15, growth is also allowed to continue until the lateral overgrowth fronts coalesce over the mask **209** at the interfaces **108d**, to form a continuous overgrown lateral gallium nitride semiconductor layer **108b**. The total growth time may be approximately 60 minutes. A single continuous growth step may be used. As shown in Figure 16, microelectronic devices **110** may then be formed in the lateral gallium nitride semiconductor layer **108a**. Microelectronic devices also may be formed in the overgrown lateral gallium nitride layer **108b**.

Finally, referring to Figures 17-22, still other embodiments of the present invention are illustrated. Figures 17-22 combine the mask **201** on the floor of the trenches **107**, as was illustrated in Figures 6-10, with the mask **209** on the top of the posts **106**, as was illustrated in Figure 11. It will be understood that the mask **201** at the bottom of the trenches, and the mask **209** on the top of the posts **106**, preferably are formed simultaneously and preferably comprise the same material. Accordingly, for example, line of sight of deposition techniques, such as thermal evaporation or electron beam evaporation of masking material such as silicon dioxide, silicon nitride and/or metal such as tungsten may be used. If the mask material is deposited after the etching step, it covers only the vertical surfaces, i.e. the top surfaces of the posts **106** and the bottom surfaces (floors) of the trenches **107**. The gallium nitride preferably nucleates little, if at all, on the masks **201** and **209**, so that gallium nitride preferably only grows from the sidewalls **105** of the posts. Alternatively, the masks **201** and **209** may comprise different materials and/or be of different thicknesses. The remaining steps of Figures 17-22 are similar to Figures 11-16, and need not be described again in detail.

It will be understood that the masks **201** may be formed on an exposed sapphire floor of the substrate **102a**, on an exposed aluminum nitride floor of layer **102b**, or on an exposed gallium nitride floor in layer **104**. Stated differently, the trenches may be etched partly into gallium nitride layer **104**, fully through gallium

nitride layer **104**, partly into aluminum nitride buffer layer **102b**, fully through aluminum nitride layer **102b**, and/or partly into sapphire substrate **102a**. Moreover, the thickness of the mask **201** may be thinner than or thicker than aluminum nitride layer **102b**. Accordingly, sapphire substrates may be used for growth of gallium nitride semiconductor layers, to thereby provide low cost and/or high availability.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

What is Claimed is:

1. A method of fabricating a gallium nitride semiconductor layer comprising the steps of:

etching an underlying gallium nitride layer on a sapphire substrate to selectively expose the sapphire substrate and define at least one post and at least one trench in the underlying gallium nitride layer, the at least one post each including a gallium nitride top and a gallium nitride sidewall, the at least one trench including a sapphire floor; and

laterally growing the gallium nitride sidewall of the at least one post into the at least one trench to thereby form a gallium nitride semiconductor layer.

2. A method according to Claim 1 wherein the etching step comprises the step of:

etching the underlying gallium nitride layer on the sapphire substrate and the sapphire substrate, to define at least one post in the underlying gallium nitride layer and in the sapphire substrate and at least one trench in the underlying gallium nitride layer and in the sapphire substrate, the at least one post each including a gallium nitride top, a gallium nitride sidewall and a sapphire sidewall, the at least one trench including a sapphire floor.

3. A method according to Claim 2 wherein the step of etching comprises the step of etching the sapphire substrate sufficiently deep to prevent vertical growth of gallium nitride from the sapphire floor from interfering with the step of laterally growing the gallium nitride sidewalls of the at least one post into the at least one trench.

4. A method according to Claim 2 wherein the sapphire sidewall height to sapphire floor width ratio exceeds about 1/4.

5. A method according to Claim 1 wherein the following step is performed between the steps of etching and laterally growing:

masking the sapphire floor with a mask that reduces nucleation of gallium nitride thereon compared to on sapphire.

6. A method according to Claim 1 wherein the etching step comprises the step of:

etching the underlying gallium nitride layer and an aluminum nitride and/or gallium nitride buffer layer on the sapphire substrate to selectively expose the sapphire substrate and define at least one post in the underlying gallium nitride layer and in the buffer layer and at least one trench in the underlying gallium nitride layer and in the buffer layer, the at least one post including a gallium nitride top, a gallium nitride sidewall and an aluminum nitride sidewall, the at least one trench including a sapphire floor.

7. A method according to Claim 6 wherein the etching step comprises the step of:

etching the underlying gallium nitride layer, the buffer layer on the sapphire substrate and the sapphire substrate to selectively expose the sapphire substrate and define at least one post in the underlying gallium nitride layer, in the buffer layer and in the sapphire substrate, and at least one trench in the underlying gallium nitride layer in the buffer layer and in the sapphire substrate, the at least one post including a gallium nitride top, a gallium nitride sidewall and a sapphire sidewall, the at least one trench including a sapphire floor.

8. A method according to Claim 1 wherein the step of laterally growing comprises the step of laterally overgrowing the gallium nitride sidewall of the at least one post onto the gallium nitride top, to thereby form a gallium nitride semiconductor layer.

9. A method according to Claim 1:

wherein the step of laterally growing is preceded by the step of masking the gallium nitride top with a mask that reduces nucleation of gallium nitride thereon compared to on gallium nitride; and

wherein the step of laterally growing comprises the step of laterally overgrowing the gallium nitride sidewall of the at least one post onto the mask, to thereby form a gallium nitride semiconductor layer.

10. A method according to Claim 1 wherein the step of laterally growing is followed by the step of forming at least one microelectronic device in the gallium nitride semiconductor layer.

11. A method according to Claim 1 wherein the step of etching is preceded by the step of forming the underlying gallium nitride layer on the sapphire substrate.

12. A method of fabricating a gallium nitride semiconductor layer comprising the steps of:

etching an underlying gallium nitride layer on a sapphire substrate to define at least one post in the underlying gallium nitride layer and at least one trench in the underlying gallium nitride layer, the at least one post including a top and a sidewall, the at least one trench including a floor;

masking the at least one floor with a mask; and

laterally growing the sidewall of the at least one post into the at least one trench to thereby form a gallium nitride semiconductor layer.

13. A method according to Claim 12:

wherein the step of etching comprises the step of etching the underlying gallium nitride layer to expose the sapphire substrate and thereby create at least one sapphire floor; and

wherein the step of masking comprises the step of masking the at least one sapphire floor with a mask that reduces nucleation of gallium nitride thereon compared to on sapphire.

14. A method according to Claim 13 further comprising the step of masking the at least one top with a mask.

15. A method according to Claim 14 wherein the steps of masking the at least one floor and masking the at least one top are performed simultaneously.

16. A method according to Claim 12 wherein the step of etching comprises the step of:

etching the underlying gallium nitride layer and an aluminum nitride and/or gallium nitride buffer layer on the sapphire substrate to define at least one post in the underlying gallium nitride layer and in the buffer layer and at least one trench in the underlying gallium nitride layer and the buffer layer, the at least one post including a top and a sidewall, the at least one trench including an aluminum nitride floor.

17. A method according to Claim 12 wherein the step of masking comprises the step of:

etching the underlying gallium nitride layer and an aluminum nitride and/or gallium nitride buffer layer on the sapphire substrate and the sapphire substrate, to define at least one post in the underlying gallium nitride layer, in the buffer layer and in the sapphire substrate and at least one trench in the underlying gallium nitride layer, the buffer layer and the sapphire substrate, the at least one post including a top and a sidewall, the at least one trench including a sapphire floor.

18. A method according to Claim 12 wherein the step of laterally growing comprises the step of laterally overgrowing the gallium nitride sidewall of the at least one post onto the gallium nitride top, to thereby form a gallium nitride semiconductor layer.

19. A method according to Claim 12:

wherein the step of laterally growing is preceded by the step of masking the gallium nitride top with a mask that reduces nucleation of gallium nitride thereon compared to on gallium nitride; and

wherein the step of laterally growing comprises the step of laterally overgrowing the gallium nitride sidewall of the at least one post onto the mask, to thereby form a gallium nitride semiconductor layer.

20. A method according to Claim 12 wherein the step of laterally growing is followed by the step of forming at least one microelectronic device in the gallium nitride semiconductor layer.

21. A method according to Claim 12 wherein the step of etching is preceded by the step of forming the underlying gallium nitride layer on the sapphire substrate.

22. A method of fabricating a gallium nitride semiconductor layer comprising the steps of:

etching an underlying gallium nitride layer on a sapphire substrate to define at least one post in the underlying gallium nitride layer and at least one trench in the underlying gallium nitride layer, the at least one post including a gallium nitride top, and a gallium nitride sidewall, the at least one trench including a trench floor; and

laterally growing the gallium nitride sidewalls of the at least one post into the at least one trench to thereby form a gallium nitride semiconductor layer;

wherein the laterally growing step is preceded by the step of treating at least one of the sapphire substrate and the underlying gallium nitride layer to prevent vertical growth of gallium nitride from the trench floor from interfering with the step of laterally growing the gallium nitride sidewalls of the at least one post into the at least one trench.

23. A method according to Claim 22 wherein the step of treating comprises the step of:

etching the sapphire substrate beneath the at least one trench sufficiently deep to create a sapphire floor and prevent vertical growth of gallium nitride from the sapphire floor from interfering with the step of laterally growing the gallium nitride sidewalls of the at least one post into the at least one trench.

24. A method according to Claim 22 wherein the step of treating comprises the step of:

masking the trench floor with a mask.

25. A method according to Claim 22 wherein the step of treating comprises the step of selectively etching the underlying gallium nitride layer to expose the sapphire substrate and create a sapphire floor.

26. A method according to Claim 22 wherein the step of laterally growing comprises the step of laterally overgrowing the gallium nitride sidewall of the at least one post onto the gallium nitride top, to thereby form a gallium nitride semiconductor layer.

27. A method according to Claim 22:

wherein the step of laterally growing is preceded by the step of masking the gallium nitride top with a mask that reduces nucleation of gallium nitride thereon compared to on gallium nitride; and

wherein the step of laterally growing comprises the step of laterally overgrowing the gallium nitride sidewall of the at least one post onto the mask, to thereby form a gallium nitride semiconductor layer.

28. A method according to Claim 22 wherein the step of laterally growing is followed by the step of forming at least one microelectronic device in the gallium nitride semiconductor layer.

29. A method according to Claim 22 wherein the step of etching is preceded by the step of forming the underlying gallium nitride layer on the sapphire substrate.

30. A gallium nitride semiconductor structure comprising:

a sapphire substrate;

an underlying gallium nitride layer on the sapphire substrate, the underlying gallium nitride layer including therein at least one post and at least one trench, the at least one post each including a gallium nitride top and a gallium nitride sidewall, the at least one trench including a sapphire floor; and

a lateral gallium nitride layer that extends laterally from the gallium nitride sidewall of the at least one post into the at least one trench.

31. A structure according to Claim 30 wherein the at least one trench extends into the sapphire substrate such that the at least one post each includes a gallium nitride top, a gallium nitride sidewall and a sapphire sidewall and the at least one trench includes a sapphire floor

32. A structure according to Claim 30 wherein the sapphire floor is free of a vertical gallium nitride layer thereon.

33. A structure according to Claim 30 wherein the sapphire sidewall height to sapphire floor width ratio exceeds about 1/4.

34. A structure according to Claim 30 further comprising:

a mask on the sapphire floor.

35. A structure according to Claim 30 further comprising:

an aluminum nitride and/or gallium nitride buffer layer between the sapphire substrate and the underlying gallium nitride layer, wherein the at least one post and the at least one trench extend through the buffer layer.

36. A structure according to Claim 30 wherein the lateral gallium nitride layer further extends onto the gallium nitride top, to thereby form a gallium nitride semiconductor layer.

37. A structure according to Claim 30 further comprising:

a mask on the gallium nitride top; and

wherein the lateral gallium nitride layer further extends onto the mask, to thereby form a gallium nitride semiconductor layer.

38. A structure according to Claim 30 further comprising at least one microelectronic device in the gallium nitride semiconductor layer.

39. A gallium nitride semiconductor structure comprising:

a sapphire substrate;

an underlying gallium nitride layer on the sapphire substrate, the underlying gallium nitride layer including therein at least one post and at least one trench, the at least one post each including a gallium nitride top and a gallium nitride sidewall, the at least one trench including a trench floor;

a mask on the at least one trench floor; and

a lateral gallium nitride layer that extends laterally from the gallium nitride sidewall of the at least one post into the at least one trench.

40. A structure according to Claim 39:
wherein the trench floor is a sapphire trench floor.

41. A structure according to Claim 39 wherein the mask is a first mask, the structure further comprising:
a second mask on the gallium nitride top.

42. A structure according to Claim 41 wherein the first mask and the second mask comprise same material.

43. A structure according to Claim 39 further comprising an aluminum nitride buffer and/or gallium nitride buffer layer between the sapphire substrate and the underlying gallium nitride layer, wherein the at least one post and the at least one trench extend into the buffer layer.

44. A structure according to Claim 39 further comprising an aluminum nitride buffer layer between the sapphire substrate and the underlying gallium nitride layer, wherein the at least one post and the at least one trench extend through the buffer layer.

45. A structure according to Claim 39 further comprising an aluminum nitride buffer layer between the sapphire substrate and the underlying gallium nitride layer, wherein the at least one post and the at least one trench extend through the buffer layer and into the sapphire substrate.

46. A structure according to Claim 39 wherein the lateral gallium nitride layer further extends onto the gallium nitride top, to thereby form a gallium nitride semiconductor layer.

47. A structure according to Claim 39 wherein the mask is a first mask, the structure further comprising:

a second mask on the gallium nitride top; and

wherein the lateral gallium nitride layer further extends onto the mask, to thereby form a gallium nitride semiconductor layer.

48. A structure according to Claim 39 further comprising at least one microelectronic device in the gallium nitride semiconductor layer.

FIG. 1

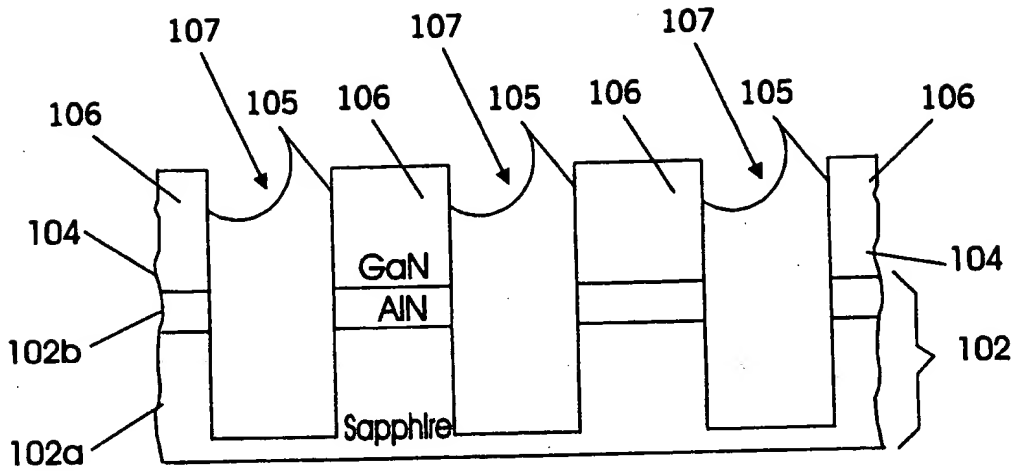
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FIG. 2

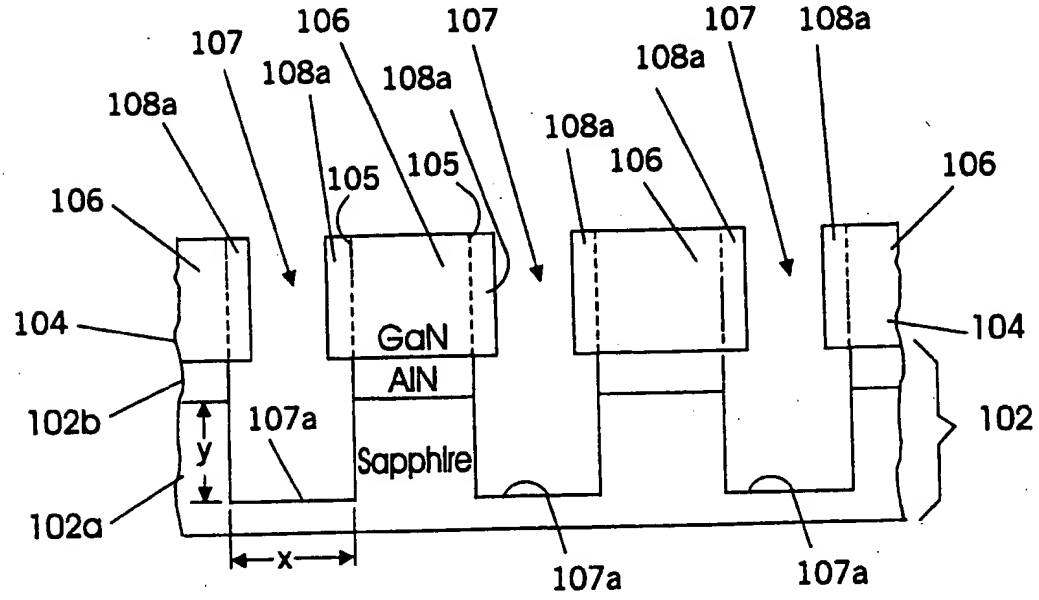
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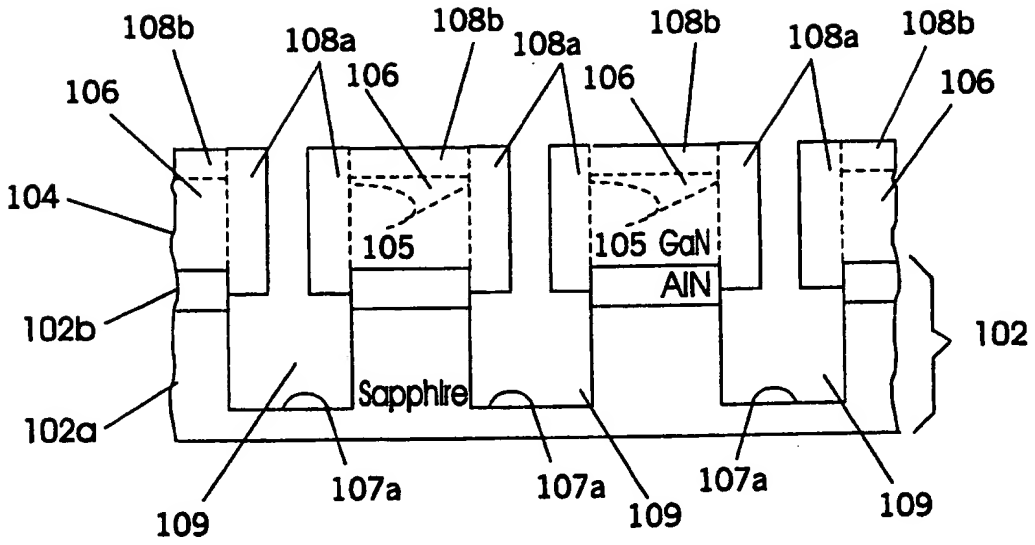
FIG. 3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107a
109

FIG. 4

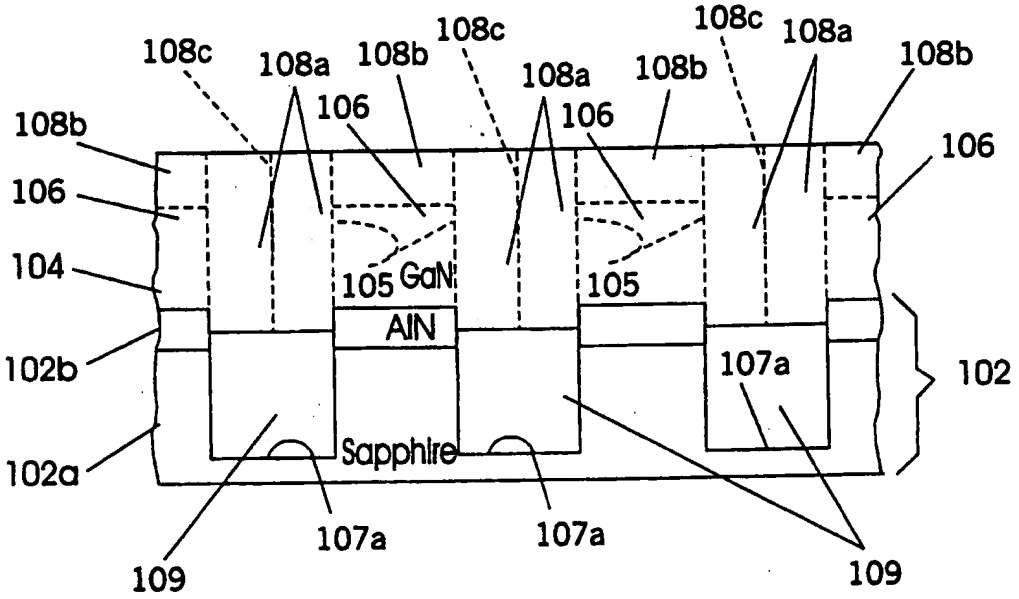
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FIG. 5

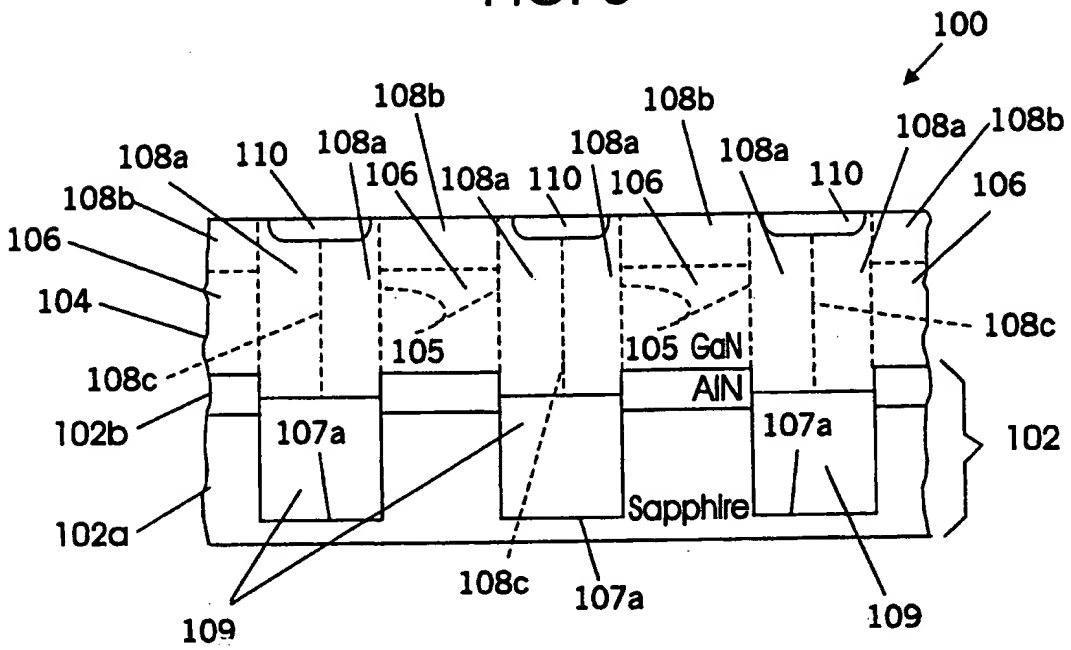
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FIG. 6

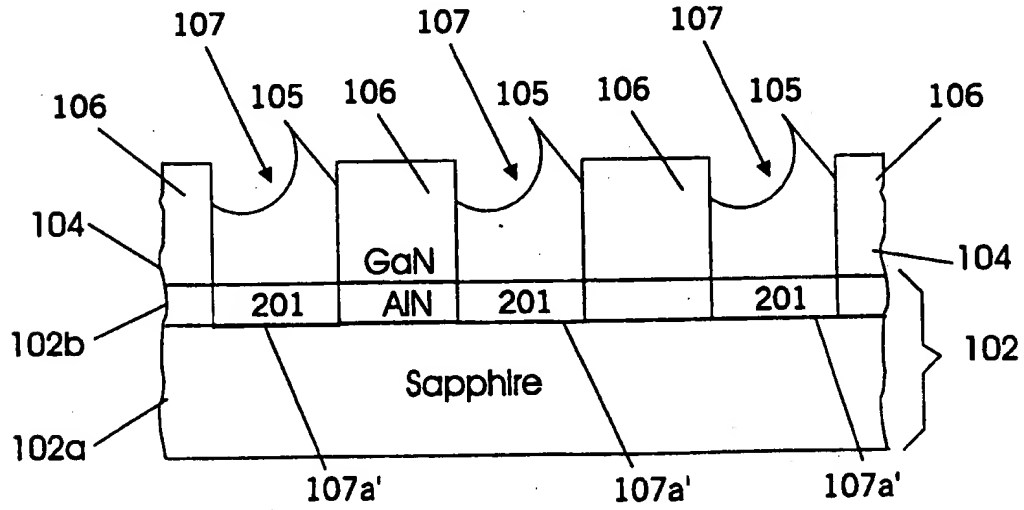
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FIG. 7

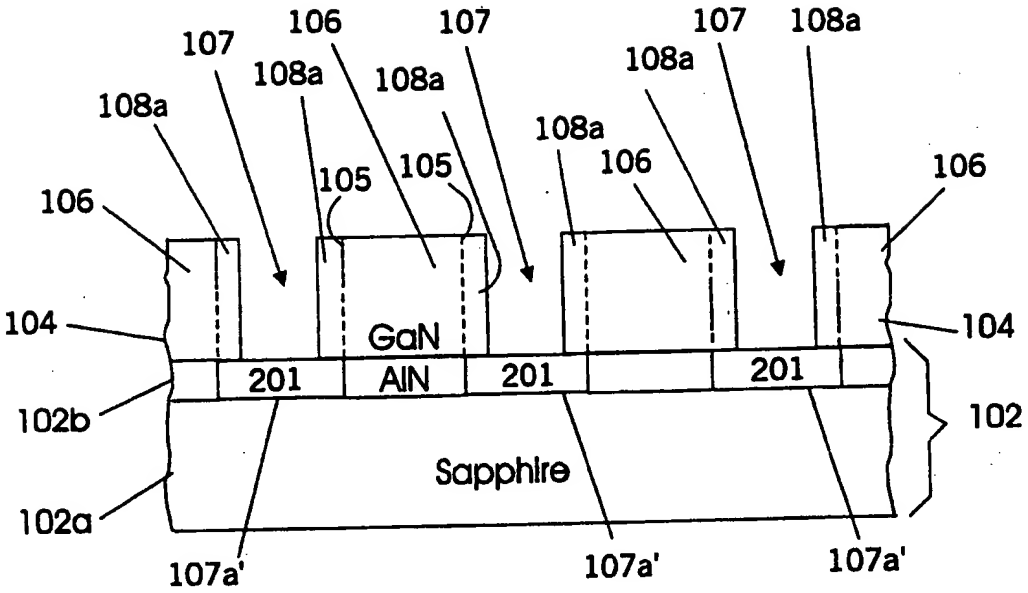
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FIG. 8

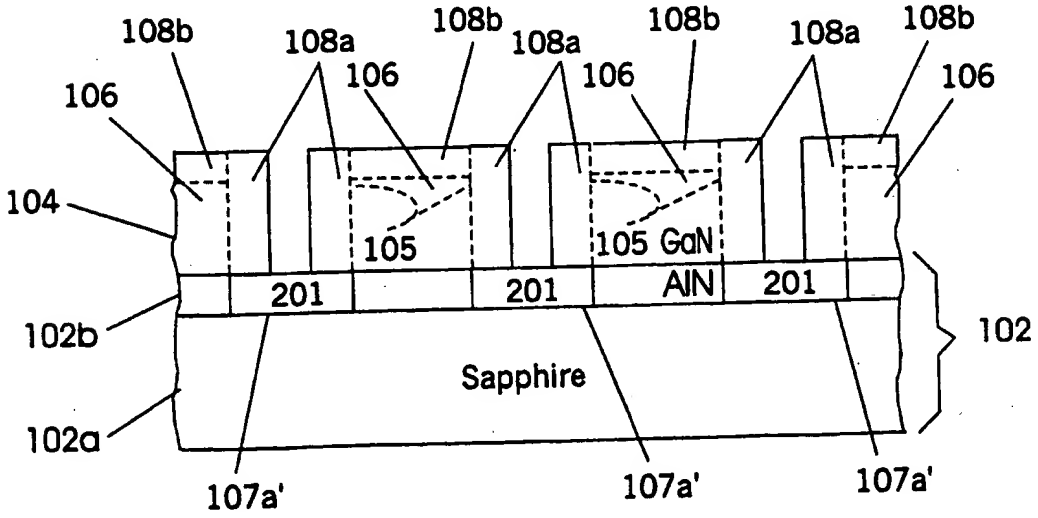
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FIG. 9

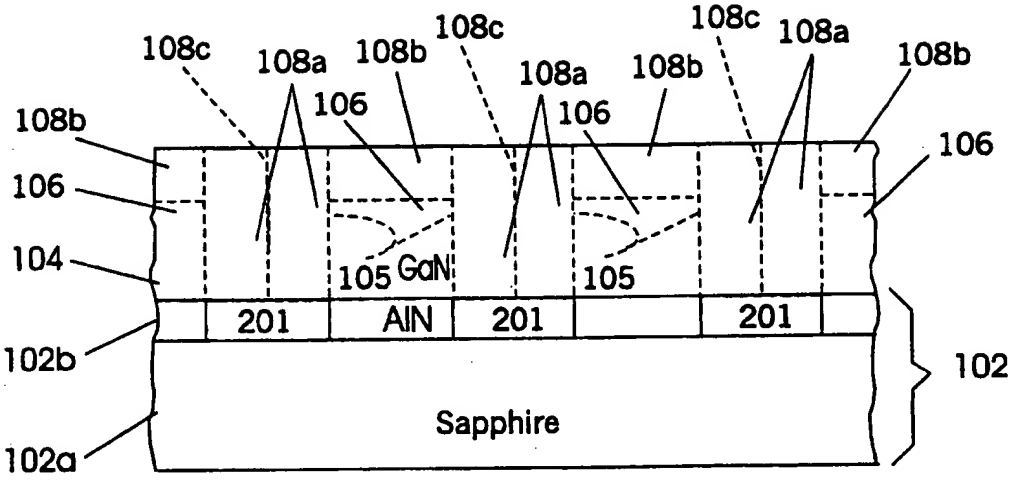
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FIG. 10

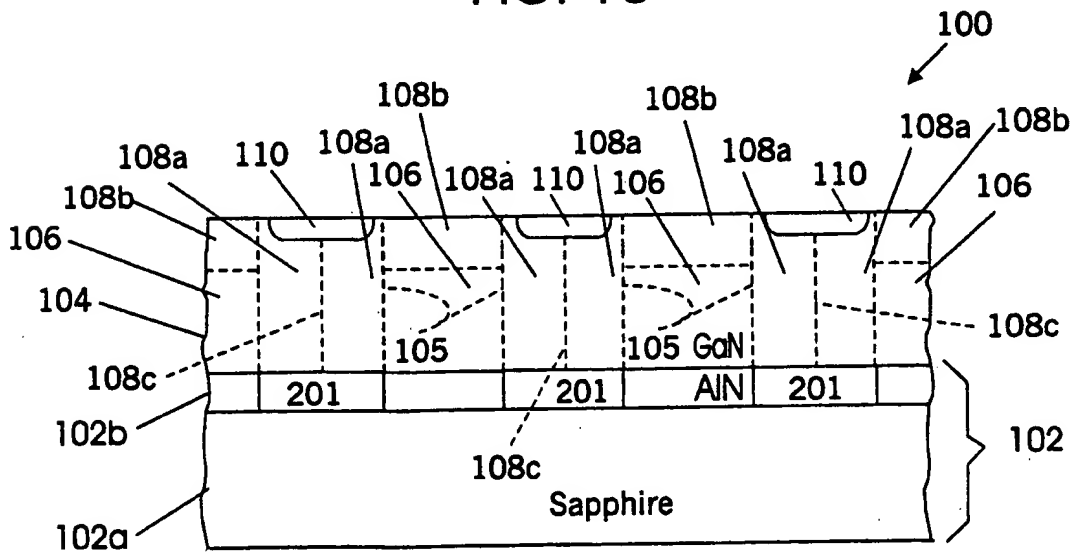
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FIG. 11

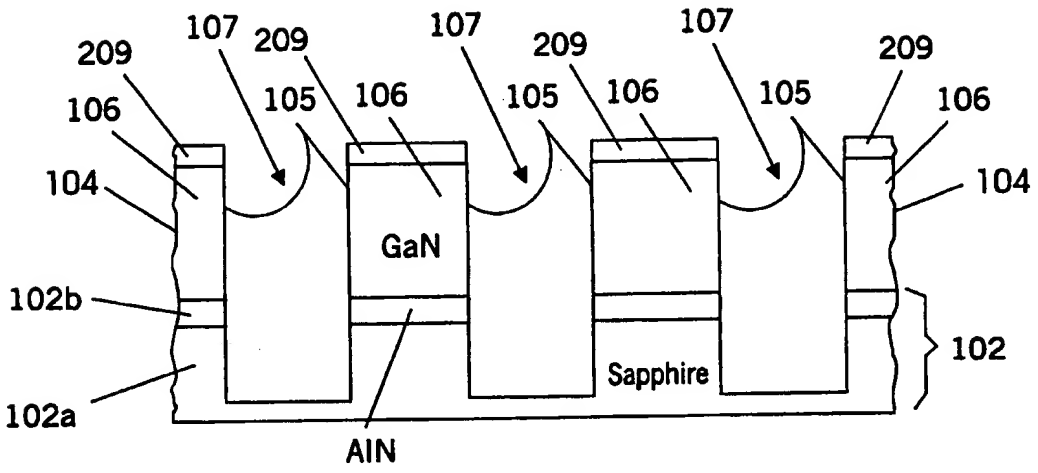
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FIG. 12

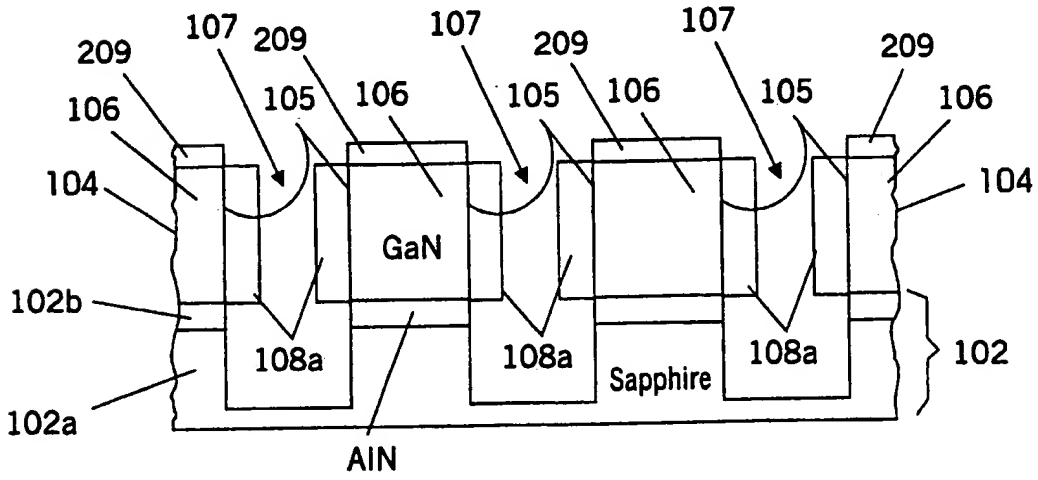
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FIG. 13

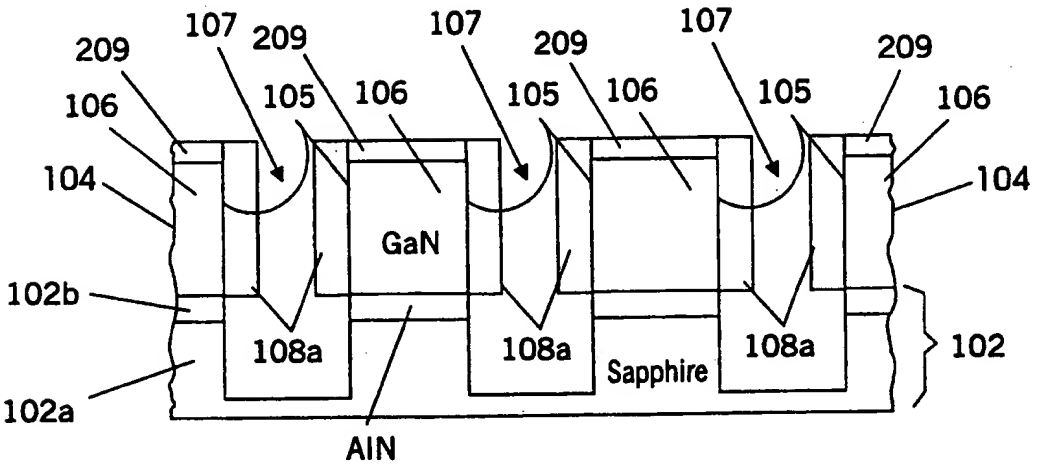
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FIG. 14

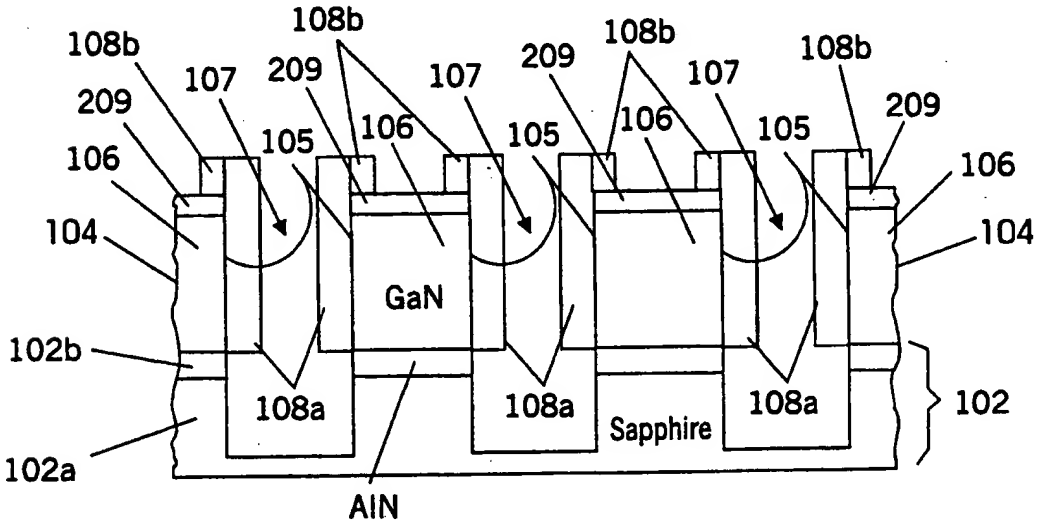
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FIG. 15

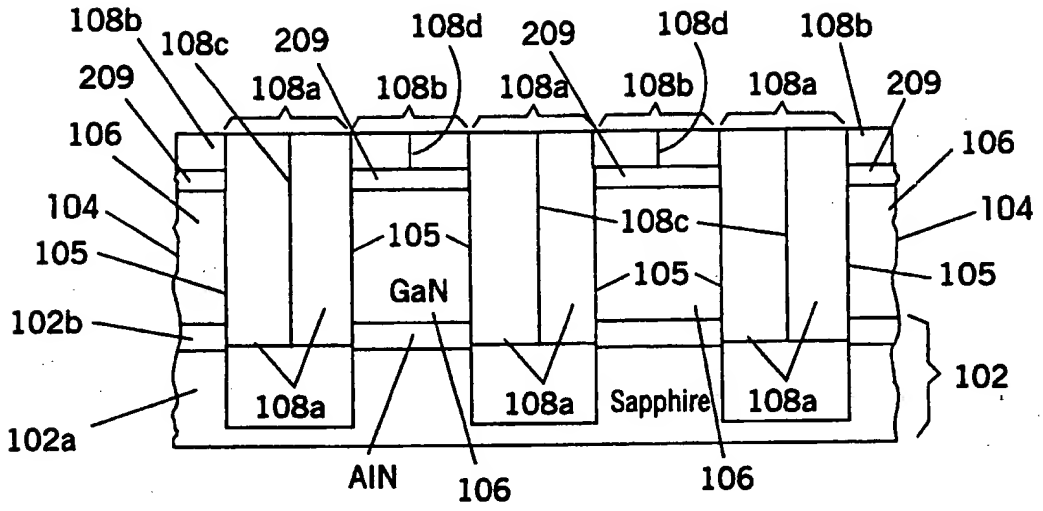
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FIG. 16

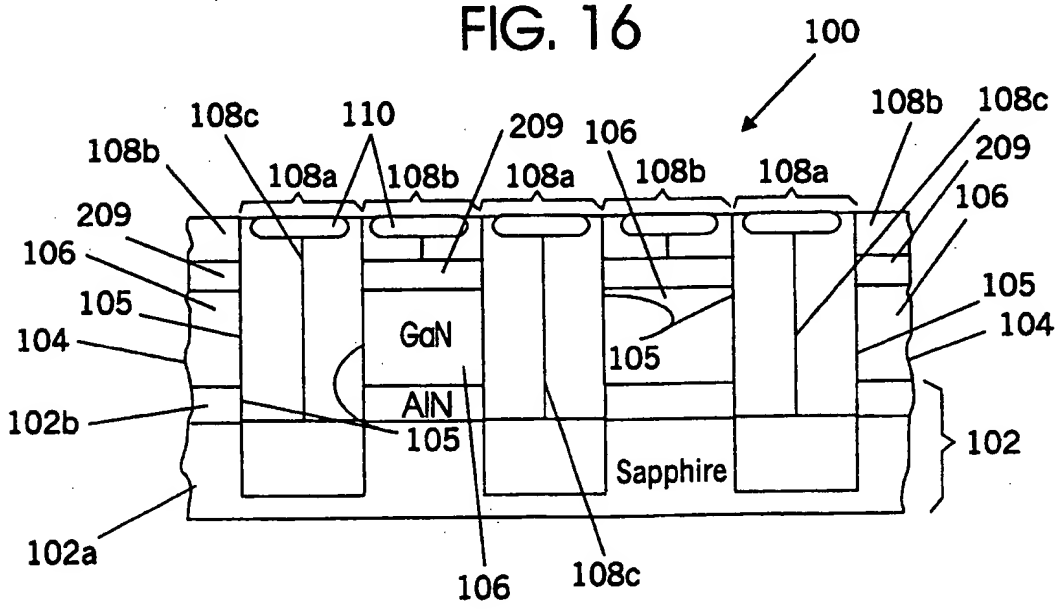
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FIG. 17

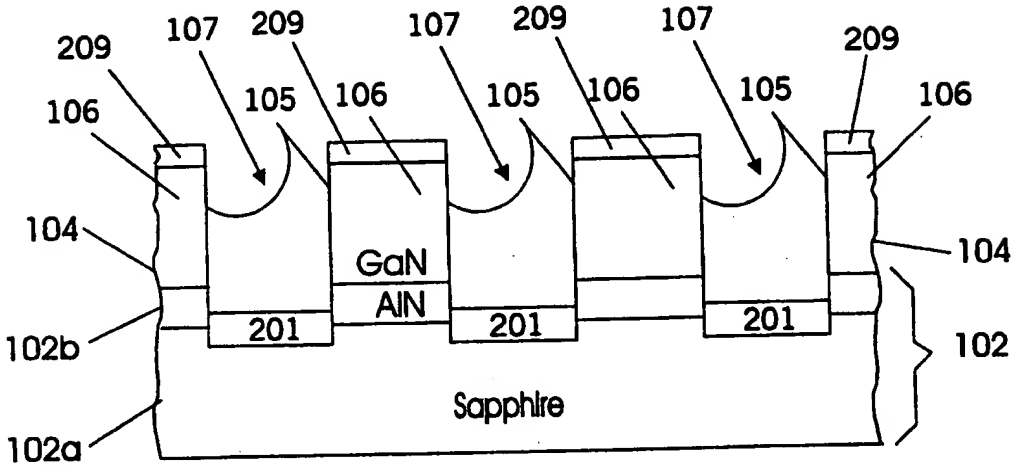
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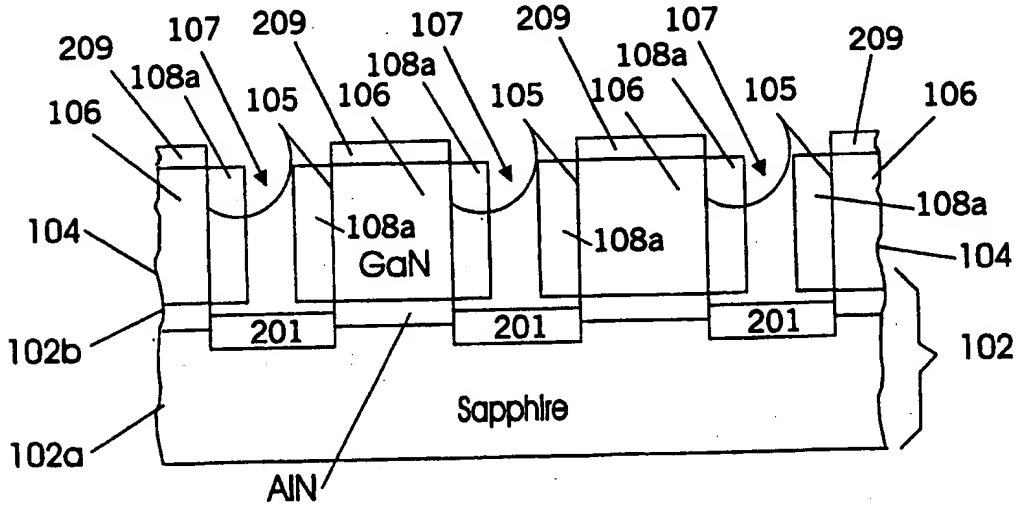
FIG. 18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105
106
105
106
105
106
104
108a
108a
104
GaN
201
201
201
102b
102
Sapphire
102a
AlN

FIG. 19

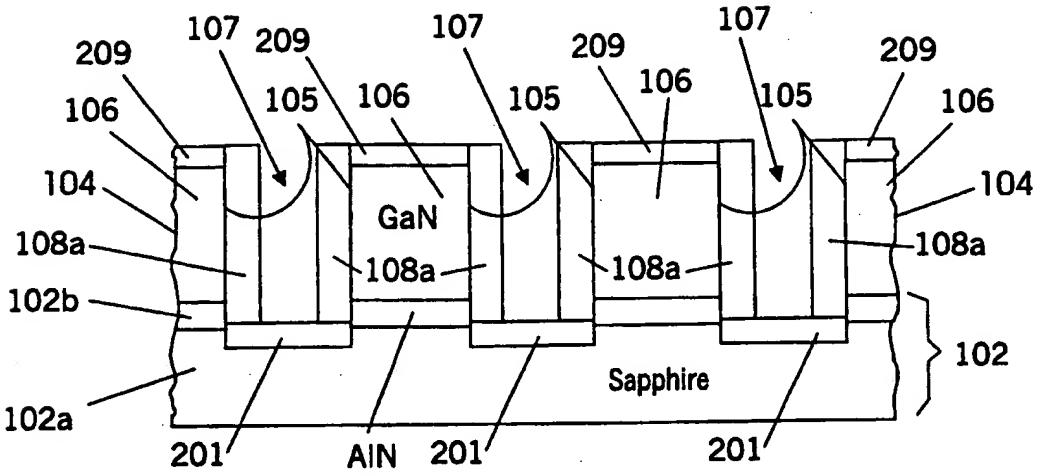

209
107
209
107
209
107
209
106
106
105
106
105
106
105
106
104
104
GaN
108a
108a
108a
108a
102b
102
Sapphire
102a
201
AlN
201
201

FIG. 20

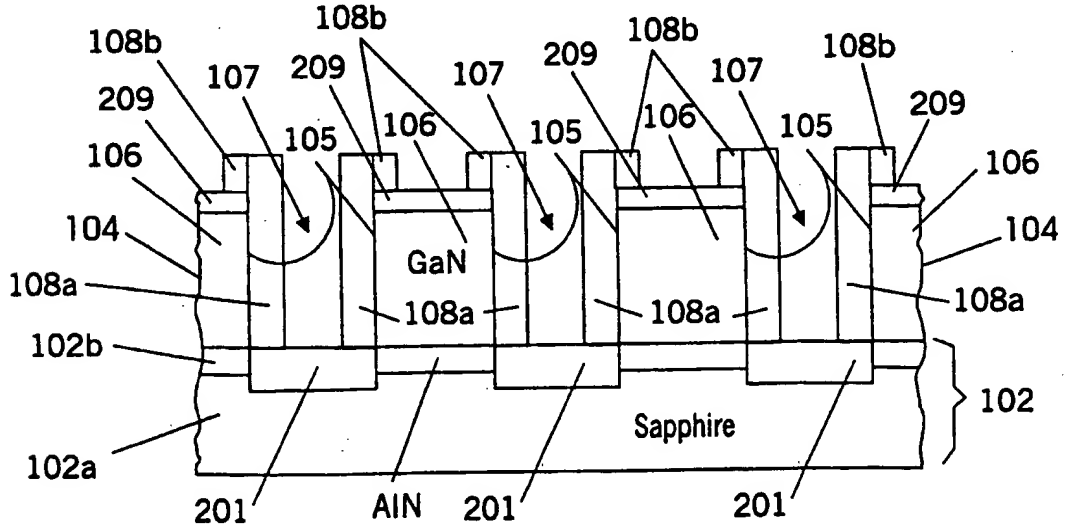
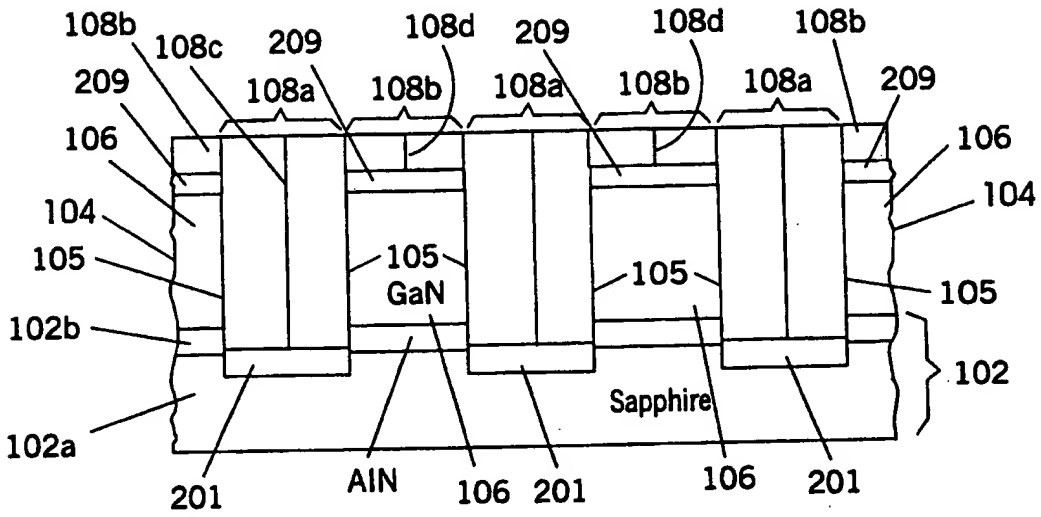

108b
108b
108b
108b
107
209
107
209
107
209
209
106
106
105
106
105
106
105
106
104
104
GaN
108a
108a
108a
108a
102b
102
Sapphire
102a
201
AlN
201
201

FIG. 21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108c
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108d
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108d
108b
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108a
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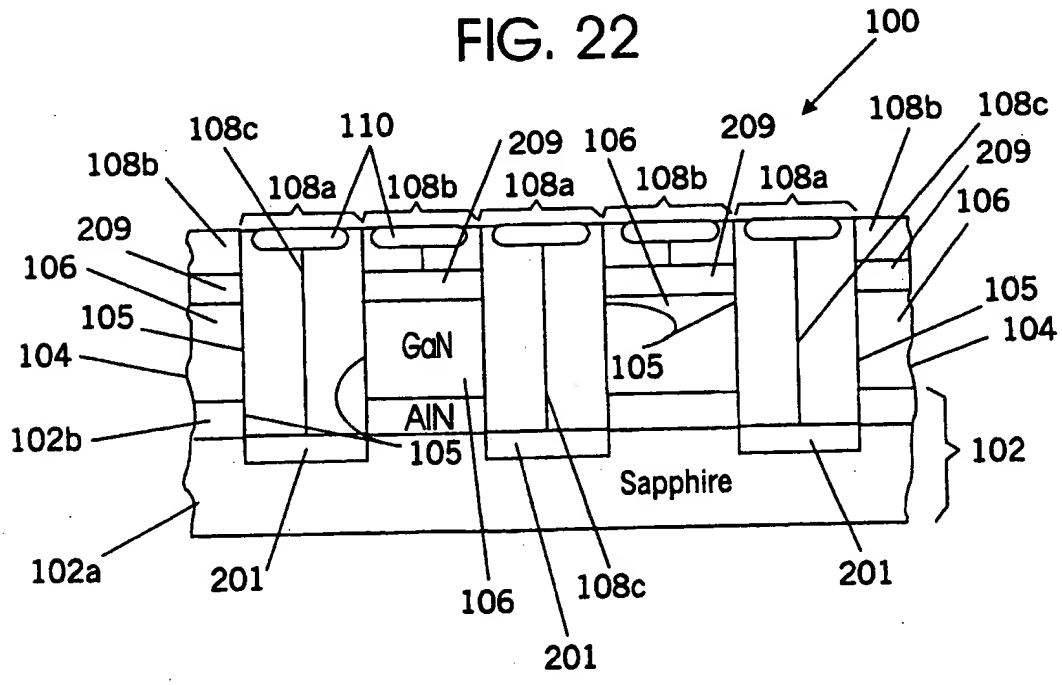
108a
108b
108a
209
106
106
104
104
105
105
GaN
105
105
102b
102
Sapphire
102a
201
AlN
106
201
106
201

FIG. 22


100
108c
110
108b
209
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209
108b
108c
108b
108a
108b
108a
108b
108a
209
209
106
106
105
105
104
GaN
104
105
AlN
102b
105
102
Sapphire
102a
201
106
108c
201
201

INTERNATIONAL SEARCH REPORT

Int ional Application No
PCT/US 00/27354

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L C30B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 942 459 A (NICHIA CHEMICAL INDUSTRIES LTD) 15 September 1999 (1999-09-15)	1,2, 5-15, 17-22, 24-32, 34-42, 44-48
A	paragraph '0062! - paragraph '0081!; figure 7; examples 35,37	3,4,16, 23,33,43

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 January 2001	24/01/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Köpf, C

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INTERNATIONAL SEARCH REPORT

Int. ional Application No
PCT/US 00/27354

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	CHEN Y ET AL: "Dislocation reduction in GaN thin films via lateral overgrowth from trenches" APPLIED PHYSICS LETTERS, vol. 75, no. 14, October 1999 (1999-10), pages 2062-2063, XP000875610 ISSN: 0003-6951	1,2,5, 8-15, 18-22, 24-32, 34, 36-42, 46-48
A	the whole document	3,4,23, 33
X	EP 0 951 055 A (HEWLETT PACKARD CO) 20 October 1999 (1999-10-20)	1,5, 8-15, 18-22, 24-30, 32,34, 36-42, 46-48
A	paragraph '0030! - paragraph '0035!; figure 3	2,23,31
P,X, L	WO 99 65068 A (NORTH CAROLINA STATE UNIVERSITY (US); ZHELEVA TSVETANKA ET AL (US)) 16 December 1999 (1999-12-16)	1-3,6-8, 10,11, 22,23, 25,26, 28-31, 35,36,38
	L: Priority page 2, line 11 -page 8, line 17; figures 1-5	

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INTERNATIONAL SEARCH REPORT

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PCT/US 00/27354

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